SPECIFICATION

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METHOD OF FORMING RETROGRADE N-WELL AND P-WELL

[h4] **Background of the Invention**

[p1] The invention relates generally to CMOS devices, and more particularly to forming discrete p- wells for the n-type devices.

[p2] In CMOS technology, it is generally known to utilize a "twin tub" process to form a discrete, p- type well region (hereafter "p-well") into which the NFET will be formed, and a discrete, n-type well region ("n-well") into which the PFET will be formed. The wells are used to more precisely control the threshold voltages of the transistors. See for example U.S. patent 5,792,680, "Method of Forming a Low Cost DRAM Cell with Self-Aligned Twin Tub CMOS Devices and a Pillar Shaped Conductor," to Sung et al. As shown in Figs. 5A-5G of the patent, an n-well and p-well are formed using a composite imaged structure of BPSG 16 and silicon nitride 18. First the p-type dopant is implanted so that it is shallower beneath the mask structure and deeper in areas where the mask structure is absent, then the n-type dopant is implanted at an energy such that it does not implant into unmasked areas. Both implants are carried out at a concentration of 1E13 to 1E14 and an energy of 1-2 Mev.

[p3] More recently, twin tub CMOS devices have utilized so-called "retrograde" wells, in which the concentration of dopant is higher at the bottom of the well and lower at the upper surface of the well. This doping profile helps prevent latch up by raising the threshold voltage of the parasitic device formed by the well. An example of prior art retrograde wells is shown in Fig. 1 of U.S. patent 5,814,866. Photoresist defines a p-well region, and a sequence of implants is carried out to form first the deep, highly doped portion of the p-well (implant concentration 1E13, energy 2 Mev), then the more shallow, more lightly doped portions of the well (e.g. 1.25 Mev, 1 Mev). Note again that a p-region forms below the mask that is shallower than where the substrate is unmasked. Then arsenic ions are implanted to form the n-well, again in a sequence with decreasing energy, to form a retrograded n-well with the mask in place.

[p4] In forming twin-tub, 0.11 um lithography CMOS devices (that is, FETs with effective channel lengths less than or equal to approximately 0.11um), the inventors found that the threshold voltages of n-type transistors within about 1.5 um of the p-well/n-well interface exhibited threshold voltage shifts of up to 80 mV. Repeated attempts to address this threshold voltage shift by altering the implant dose and/or energy proved unsuccessful. While these threshold voltage shifts could be reduced to some extent by altering doping profiles, they were not eliminated or reduced to an acceptable level (i.e. less than about 10 mV). Moreover, these solutions created new problems. The altered doping profiles decreased the efficiency of the resulting well regions. These shifts in threshold voltage could lead to catastrophic failures in the Boolean operations of the resulting logic circuits.

[h5] **Brief Summary of the Invention**

[p5] It is thus an object of the present invention to form twin-tub CMOS devices that do not exhibit threshold voltage shifts in devices adjacent the p-well/n-well interface.

[p6]   In a first aspect, the invention comprises a method of forming the n-well and p-well regions on a substrate, comprising the steps of forming a first mask structure having a given thickness on the substrate; carrying out n-well implants into regions of the substrate exposed by the first mask structure; substantially reducing said thickness of said first mask structure; carrying out a first p-well implant through said first mask structure, so that a first implant region is formed below the n-well and a second implant region is formed below the first mask structure, the first implant region being deeper than the second implant region; forming a second mask structure on the substrate having an image generally complementary to the first mask structure; and carrying out p-well implants into regions of the substrate exposed by the second mask structure.

[p7]   In a second aspect, the invention comprises a method of forming abutting retrograde n-well and p-well regions on a substrate, comprising the steps of forming the retrograde n-well by implanting with a first dopant species; and forming the retrograde p-well by first carrying out a deep implant with a second dopant species under conditions that substantially reduce scattering of said second dopant species into abutting regions of said retrograde n-well.

[p8]   In a third aspect, the invention comprises a CMOS device having FETs with effective channel lengths less than or equal to approximately 0.11um formed in adjacent, retrograde nwells and pwells, wherein threshold voltages of FETs formed with approximately 1.5 um of an interface between said nwells and pwells are constant within approximately 10 mV.

[h6]   **Brief Description of the Several Views of the Drawings**

[p9]   The foregoing and other aspects of the invention will be described in more detail below with reference to the accompanying drawing, in which Figs.1-5 are cross sectional views of a semiconductor substrate fabricated in accordance with a preferred embodiment of the

present invention.

[h1] Detailed Description of the Invention

[p10] In further investigations, the present inventors determined that these threshold shifts (within approximately 1.5 um of the p-well/n-well interface) were due to scattering of boron ions during the formation of the deep, heavily-doped portion of the retrograde p-well. Specifically, it was determined that the photoresist mask scattered boron ions off-vertical into adjacent portions of the n-well. Therefore, the inventors established the present process, which provides appropriate masking for the respective wells during formation, but does not induce boron scattering during the deep well implant.

[p11] With reference to Fig. 1, a 200 nanometer (nm) layer of polycrystalline silicon (polysilicon) 12 is deposited on a semiconductor substrate 10. The substrate 10 can be silicon, silicon-germanium, gallium arsenide, or any other semiconductor base in which CMOS devices can be formed. Typically the twin tubs are formed in the substrate 10 after isolation regions (for example, shallow trench isolation) have been formed, but these are not shown in the drawing for ease of illustration. Further, immediately prior to the sequence of steps described herein a thin oxide (for example, if the substrate is silicon, silicon oxide about 60 angstroms thick) is preferably grown on the substrate; again, for ease of illustration this thin protection layer is not shown. The polysilicon layer 12 can be made of other materials (such as silicon nitride and silicon oxide) that can be deposited and etched in the same manner as the polysilicon layer 12, as described in more detail below. The polysilicon layer 12 is preferably of a thickness of approximately 100-300nm. Other thicknesses could be used.

[p12] A 2000nm thick layer of photoresist 14 is then deposited and patterned on substrate 10, to provide photomask 14 as shown in Fig. 2. Note that at this juncture, the polysilicon 12 is

not patterned. This is so it can protect substrate 10 from damage during the ion implantation steps described below. As a result, a combined masking structure of 2000nm of photoresist 14 and 200nm polysilicon 12 define an area of the substrate where the n-well is to be formed. In practice the photoresist layer 14 is typically 1800-2500nm in thickness. Other thicknesses could be used.

[p13] Subsequently, as shown in Fig. 3, a series of implant steps are carried out to define the retrograde n-well 16, comprising a deep high dose implant 16C at a energy of 850,000 electron volts, and a dosage of 5.2 times 10 to the 13th energy per square centimeter (as abbreviated hereafter, 850 kEv, 5.2 x 10 e 13 per cm2), intermediate dose implant 16B (550 kEv, 1.25 x 10 e 12 per cm2) and low dose implant 16A (50 kEv, 5 x 10 e 11 per cm2), all of phosphorous (arsenic could also be used, with appropriate changes in the doses and energies). Note that during this set of implant steps the photoresist is thick enough to prevent ions from substantially penetrating through the polysilicon layer 12. A final, shallower implant could also be carried out to more precisely control dopant levels at the surface of substrate 10. Obviously the powers and dosage densities can be varied, so long as the overall implant profile (featuring deep high dose implant, intermediate dose implant, and shallow lower dose implant) is provided. Moreover, additional implants could be added.

[p14] Then, as shown in Fig. 4, the exposed portion of the layer 12 is removed (preferably by reactive ion etching in a bromine or chlorine-based ambient), and photoresist 14 is removed by plasma etching in an oxygen environment., so that a portion of the polysilicon layer 12 remains. Then a boron implant is done at 550 kEv, 2.5 x 1.0 e 14 per cm2 to form a deep p-type implant region 18C. The present inventors have found that by doing this deep implant in the presence of a relatively thin masking material (the 200nm polysilicon 12), boron scattering during this implant step is substantially eliminated. The threshold voltages of the NFETs formed in the p-well do not vary as a function of distance from the p-well/n-well interface. Specifically, experimental results showed that threshold voltage shifts of FETs formed within approximately 1.5 um of the interface between the n-well

and the p-well, as compared to FETs formed elsewhere, were either zero or negligible (not greater than 10mV). Note also that this dosage and energy of boron results in a portion of region 18C immediately below the deepest n-well implant 16C, which decreases junction capacitance and hence enhances the switching speed of the resulting transistors.

[p15] Finally, as shown in Fig. 5, the polysilicon layer 12 is stripped, a new photoresist between 1800-2500nm is deposited and imaged to form a second implant blocking mask 20,. An intermediate dose implant 18B (150 kEv, $1.25 \times 10 e 12$ per cm2) and low dose implant 18A (45 kEv, $5 \times 10 e 11$ per cm2) are provided to define the retrograde p-well 18. Again, a final, shallower implant could also be carried out to more precisely control dopant levels at the surface of substrate 10. Again, the dosages and number of implants can be varied as in the case of the n-well 16 as described above. The inventors found that at these dosages and powers there was no evidence of boron scattering, hence the thicker implant blocking mask 20 can be used. FETs (not shown) are subsequently formed in the respective wells to provide the final CMOS device.

[p16] As will be apparent to those of ordinary skill in the art, various modifications may be made to the structures and teachings set forth above without departing from the spirit and scope of the invention as described and claimed. For example, polysilicon 12 can be made of other materials and can be other thicknesses. Moreover, materials other than conventional photoresist could be used to provide the thick implant mask, such as other cross linkable polymers such as polyimide. Finally, instead of forming the mask structure from two separate layers, the results of the invention could be achieved by using a single layer that is thick when carrying out the n-well implants and is then thinned to carry out the deep p-well implant. As a practical matter such an alternate embodiment would not include retaining a portion of the masking layer to prevent implant damage during formation of the n-well.